REMARKS

Claims 1-23 are currently pending. Claims 1, 11 and 21 have been amended. No new matter has been added.

Claim Rejections Under 35 U.S.C. §112

Claims 1-23 were rejected under 35 U.S.C. §112, second paragraph, for indefiniteness. In response, these claims have been amended to comply with 35 U.S.C. §112, second paragraph. Thus, Applicant respectfully requests reconsideration of these claims and withdraw of the rejections.

Claim Rejections Under 35 U.S.C. §102

Claims 1-5, 11-15 and 21-23 were rejected under 35 U.S.C. §102(a) as anticipated by Masatake (JP 2003-202362).

Applicant respectfully traverses.

Independent claim 1 recites the following limitations:

scanning a first test data from an input pin into a first scan chain during a first state of a clock cycle; and

scanning a second test data from the input pin into a second scan chain during a second state of the clock cycle;

wherein a clock signal of the clock cycle is directly input to the first scan chain and the second scan chain during testing.

Applicant respectfully submits that Masatake does not disclose or suggest each and every limitation of the present claims.

In FIG. 1, Masatake is directed to a scanning test circuit having scan chains 11, 12, which consist of series-connected circuits of two or more flip-flops for testing internal circuitry. According to Masatake, scanning test data and a scanning clock are inputted at the time. The 1st shift register (1st scan chain) 11 operates with synchronizing a 1st edge (starting) of the scanning clock, and the 2nd shift register (2nd scan chain) 12 operates with synchronizing a 2nd edge (falling) of the scanning clock. The two scanning chains (1st and 2nd shift registers) 11, 12 operate on the rising edge and falling edge of the scanning clock.

In FIG. 2, Masatake discloses the configuration for the 1st and 2nd shift registers (1st and 2nd scan chains) 11, 12. According to Masatake, shift registers (scan chains) 11, 12 show a plurality of flip-flops (F/F) 111, 112, ..., 11n from which each is a latch (flip-flop) holding 1-bit data and constitutes the shift register of n (positive integer) bit. This configuration has internal circuitries 121, 122, ..., 12m of m (positive integer) individual for a scanning test, and an AND gate 131 that outputs the logical AND of the scanning enable input signal EN and the scanning clock input signal CLK as a shift clock CK.

As shown in FIG. 2, Masatake explicitly discloses that the enable (EN) signal and the original clock (CLK) signal must be supplied as the input to the AND gate 131 so that the AND gate 131 provides the shift clock (CK) signal to the flip-flop circuits 111, 112, ..., 11n. According to Masatake, for each of the 1st and 2nd scan chains 11, 12, the original clock (CLK) signal must pass through AND gate 131 along with enable (EN) signal prior to being provided as an input to the flip-flops of each scan chain 11, 12. As is generally known in the art and conformed by Masatake and the Action, a scan chain is a plurality of series connected flip-flops, such as flip-flops 111, 112, ..., 11n. This explicit disclosure by Masatake teaches away from what is claimed by the Applicant in the present claims, because the original clock (CLK) signal of Masatake is not input directly to the flip-flops 111, 112, ..., 11n of the1st and 2nd scan chains 11, 12.

In contrast, the present claims recite that the clock signal is directly input to the first scan chain and the second scan chain during testing. Masatake does not disclose or even suggest this feature of the present claims.

For at least these reasons, it is respectfully submitted that independent claim 1, as amended, is not anticipated by the cited Masatake reference.

For at least these same reasons, it is respectfully submitted that independent claims 11 and 21, as amended, are likewise not anticipated by this reference.

Since the remaining claims respectively depend from these independent claims, these dependent claims are considered allowable over this reference for at least the same reasons as discussed above.

Claim Rejections Under 35 U.S.C. §103

Claims 8 and 18 were rejected under 35 U.S.C. §103(a) as unpatentable over Masatake (JP 2003-202362).

Claims 6, 9, 16 and 19 were rejected under 35 U.S.C. §103(a) as unpatentable over Masatake in view of Jaramillo ("10 Tips for Successful Scan Design", 2/17/2000).

Claims 7, 10, 17 and 20 were rejected under 35 U.S.C. §103(a) as unpatentable over Masatake in view of Jaramillo and Morton (US 2004/0078741).

However, Applicant respectfully traverses these rejections under 35 U.S.C. §103(a) for at least the reasons as set forth above in response to the 35 U.S.C. §102(a) rejections.

Since claims 6-10 and 16-20 respectively depend from independent claims 1, 11 and 21, these dependent claims are considered allowable over the cited references for at least the same reasons as discussed above and/or for at least their dependence on the independent claims.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Bingham McCutchen's Deposit Account No. **50-2518**, referencing billing number **7035962001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. **50-2518**, referencing billing number **7035962001**.

Respectfully submitted,
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